THAT WHICH IS CLAIMED IS:

1. A control circuit for a PWM regulator circuit for use in switching power supplies, the regulator circuit being adapted to receive, as an input, a square-wave voltage signal with a predetermined duty cycle and to supply, as an output, a regulated direct-current voltage, and comprising a switching device adapted to modulate the duty cycle of the input signal, the control circuit comprising:

detector means for detecting the trailing edges of the voltage signal input to the regulator circuit and adapted to emit a reset pulse coinciding with each of the said edges;

ramp signal generator means, coupled to the detector means and adapted to generate a voltage signal with a linearly variable amplitude and to reset the signal upon receipt of a reset pulse;

first comparator means to be connected to the output of the regulator circuit and adapted to compare the voltage signal present at the output with a reference voltage signal, and to emit a voltage-error signal in relation to the outcome of the comparison;

second comparator means adapted to compare the ramp signal with the error signal and to emit a pulse-width modulated signal in dependence on the outcome of the comparison; and

driver means for driving the switching device of the regulator circuit, the driver means being adapted to receive the pulse-width modulated signal and to emit a driving signal for driving the device in order to control its conduction interval;

wherein the ramp-signal generator means is arranged to trigger the generation of the signal at a

moment coinciding with the leading edge of the voltage signal input to the regulator circuit;

the driving signal for the switching device having a duty cycle less than or equal to the duty cycle of the signal input to the regulator circuit, with modulation of the leading edge over time and with the trailing edges coinciding.

2. A circuit according to Claim 1, wherein the first comparator means comprise an error amplifier having its inverting input connected to a source of a reference voltage signal, its non-inverting input being intended for connection to the output of the regulator circuit.

3. A circuit according to Claim 1, wherein in the second comparator means, the ramp-voltage signal is applied to the non-inverting input and the voltage-error signal is applied to the inverting input.

4. A circuit according to Claim 3, wherein the second comparator means emits a positive square-wave signal when the ramp signal is greater than the error signal.

5. A circuit according to Claim 1, wherein the driver means comprise a bistable circuit the set input of which is connected to the output of the second comparator means and the reset input of which is connected to the output of the detector means.

6. A circuit according to Claim 5, wherein the reset input of the bistable circuit is coupled to the output of the detector means via a delay line.

7. A circuit according to Claim 5, wherein the bistable circuit is an S-R flip-flop.